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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/636,087	SAVELL, THOMAS C.	
	Examiner	Art Unit	
	Joseph Saunders	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62 and 64-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62 and 64-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the communications filed June 7, 2007.

Claims 1 – 62 and 64 – 71 are currently pending and considered below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 68 and 69 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 68 and 69 state "the machine-readable medium of claim 45" however claim 45 is directed to "a method of processing media data" and since claim 68 is substantially similar in scope to claim 45 and claim 69 is substantially similar in scope to claim 46 it is believed that the Applicant intended claims 68 and 69 to depend on claim 47 and therefore will be examined as if this was the case. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 1 – 18, 20 – 62, and 64 – 71 are rejected under 35 U.S.C. 102(e) as being anticipated by Borland et al. (US 6,724,772 B1), hereinafter Borland.

Claim 1: Borland discloses a digital processing integrated circuit to process media data (integrated circuit 100 data transfers may be voice, audio, and/or video, Column 5 Lines 43 – 45 and Figures 1 – 3), the integrated circuit including: a plurality of processing modules to process the media data (modules 210A – 210H); a data path to communicate data between the processing modules, wherein the data path is arranged within the integrated circuit in a ring configuration (two circular buses, 330 and 332) wherein each processing module of the plurality of processing modules is configured to communicate the media data to an adjacent processing module (Since processing modules are arranged in a ring configuration the data must be passed to an adjacent processing module) and media data is clocked from processing module to processing module around the data path so as to communicate from a source processing module to a target processing module (Since the modules are serially connected the modules and the bus is a TDMA bus, data is passed through all modules starting with the source however is only processed at the appropriate destination module, Column 1 Line 39 – Column 2 Line 44 and Column 5 Lines 55 – 59); and a digital interface to communication with a device external to the integrated circuit (module 210 may be an I/O controller communicating with a computer system) (Column 1 Lines 5 – 35, Column 3 Line 64 – Column 4 Line 12).

Claim 2: Borland discloses the integrated circuit of claim 1, wherein the data path defines a media data path including a digital audio bus that interconnects the plurality of

processing modules in series ("Buses 330 and 332 may be serial or parallel buses, as desired," Column 6 Lines 24 – 36. Further the modules are arranged in a circular configuration and there is only one common media data path. Therefore the processing modules are arranged in series).

Claim 3: Borland discloses the integrated circuit of claim 2, wherein the digital audio bus communicates digital audio data in a plurality of time-slots ("The bus controller 350 may enable data transfers on the TDMA bus 330 only during assigned time slots of assigned frequency and assigned length," Column 5 Lines 55 – 59), each particular processing module having at least one programmable or fixed time-slot from which data is received from the data path for processing by the particular processing module ("The schedule includes information on time slot assignments for one or more of the plurality of modules," Column 6 Lines 6 – 11) and wherein media data corresponding to different processing modules is present at the same time on the data path (Since this is TDMA system media data corresponding to different processing modules is present in different time slots or "at the same time" referring to absolute time, on the data path, Column 5 Lines 55 – 59).

Claim 4: Borland discloses the integrated circuit of claim 2, wherein the digital audio bus communicates digital audio data in a plurality of time-slots, each particular processing module being assigned at least one time-slot into which data processed by the particular processing module is exported to the digital audio bus ("If the timing

indicates real-time or fast response, then the bus controller 350 may assign multiple contiguous time slots to the data transfer associated with that request. Time slots may be set with any frequency and/or length, as desired," Column 6 Lines 1 – 5) and wherein media data corresponding to different processing modules is present at the same time on the data path (Since this is TDMA system media data corresponding to different processing modules is present in different time slots or "at the same time" referring to absolute time, on the data path, Column 5 Lines 55 – 59).

Claim 5: Borland discloses the integrated circuit of claim 3, wherein one of the processing modules is a Digital Signal Processor (DSP) (bus controller 350) and the data path communicates processing control data in a plurality of time-slots that are allocated to the processing modules under control of the DSP ("the bus controller 350 includes, or has direct access to, a memory 315, which stores a schedule of the data transfers." "The bus controller examines the schedule when a new request is received and allocated unused time slots for the new request," Column 6 Lines 6 – 24).

Claim 6: Borland discloses the integrated circuit of claim 1, wherein the data path is a time division multiplexed bus ("bus 330 is a time division, multiple access (TDMA) bus", Column 5 Lines 55 – 59) including a plurality of audio channels (time slots for audio data).

Claim 7: Borland discloses the integrated circuit of claim 1, wherein the data path communicates data between the plurality of processing modules at bit rates that differ ("If the timing indicates real-time or fast response, then the bus controller 350 may assign multiple contiguous time slots to the data transfer associated with that request. Time slots may be set with any frequency and/or length, as desired," Column 6 Lines 1 – 5).

Claim 8: Borland discloses the integrated circuit of claim 7, wherein the media data path includes a total number of time-slots for communicating media data at a plurality of different bit rates, and wherein the sum of a number of time-slots allocated to each one of the plurality of bit rates equals the total number of time-slots summed across every bit rate ("If the timing indicates real-time or fast response, then the bus controller 350 may assign multiple contiguous time slots to the data transfer associated with that request. Time slots may be set with any frequency and/or length, as desired," Column 6 Lines 1 – 5. Therefore, the sum of a number of time-slots allocated to each one of the plurality of bit rates equals the total number of time-slots summed across every bit rate).

Claim 9: Borland discloses the integrated circuit of claim 1, wherein the plurality of processing modules are connected in series ("Buses 330 and 332 may be serial or parallel buses, as desired," Column 6 Lines 24 – 36. Further the modules are arranged in a circular configuration and there is only one common media data path. Therefore the processing modules are arranged in series) and each processing module is configured

to: selectively extract media data for processing from the data path, the media data being provided in at least one time-slot (TDMA, Column 5 Lines 55 – 59) of the data path allocated to the processing module; selectively insert processed media data into its allocated time-slot; and pass media data that it receives and that is associated with other processing modules unchanged along the data path (Data is passed from module to module in a manner controlled by the bus controller and task specific or task general processing takes place at each module, Column 4 Lines 1 – 5, Column 6 Lines 24 – 35).

Claim 10: Borland discloses the integrated circuit of claim 1, wherein the number of processing modules connected along the data path is configurable, each processing module included in the device being allocated at least one time-slot provided by the data path (Borland discloses that the integrated circuit 100 contains "a plurality of modules 210," Column 5 Lines 14 – 19, and therefore allows for the number of modules to be configurable).

Claim 11: Borland discloses the integrated circuit of claim 1, wherein the data path includes a control data path ("integrated circuit 100 includes a unified data, address, and control bus 330, or a separate data bus 330 and control bus 332," Column 6 Lines 24 – 36) to communicate processing control data (transfer requests) to at least one processing module, the processing control data being used by the processing module to process digital data received from the data path (Transfer requests provide identifier

information, transfer size, and timing information necessary for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36).

Claim 12: Borland discloses the integrated circuit of claim 11, wherein the processing control data includes parameters for digital signal processing by the processing module (Transfer requests provide identifier information, transfer size, and timing information necessary for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36).

Claim 13: Borland discloses the integrated circuit of claim 12, wherein the parameters include at least one of filter parameters, time delay parameters ("The bus controller examines the priority value and the timing value when the bus controller analyzes the request for transfer," enabling for example previously scheduled requests to be reassigned or delayed to later time slots, as necessary, Column 6 Lines 6 – 23. This information is provided in the transfer requests or control data.), mixing parameters, or sample-rate conversion parameters.

Claim 14: Borland discloses the integrated circuit of claim 11, wherein the control data path ("integrated circuit 100 includes a unified data, address, and control bus 330, or a separate data bus 330 and control bus 332," Column 6 Lines 24 – 36) is a time division multiplexed bus arranged to interconnect the plurality of modules in the ring configuration (Figures 2 and 3) and wherein while the media data is communicated from

the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path (Since the modules are serially connected the modules and the bus is a TDMA bus, data is passed through all modules starting with the source however is only processed at the appropriate destination module, Column 1 Line 39 – Column 2 Line 44 and Column 5 Lines 55 – 59).

Claim 15: Borland discloses the integrated circuit of claim 11, wherein the processing control data includes streams of processing control data each of which is associated with a stream of media data communicated via the data path, each stream of processing control data being destined for an associated target processing module to which the stream of media data is communicated ("Streams" of data are communicated in time slots on buses 330 and 332 and the buses may be serial or parallel, the control data is associated with the media data and tells the associated target processing module how to process the media data, Column 1 Line 39 – Column 2 Line 44).

Claim 16: Borland discloses the integrated circuit of claim 15, wherein each stream of processing control data is arranged to be communicated via the control data path to arrive at its associated target processing module prior to a source processing module exporting the media data to the media data path ("bus controller examines the priority value and the timing value when the bus controller analyzes the request for the transfer," Column 6 Lines 21 – 23).

Claim 17: Borland discloses the integrated circuit of claim 1, wherein the data path includes: a plurality of media channels (time slots for audio data) defined by time division multiplexed time-slots; and a channel identification path (address bus) including channel identification data ("an identifier which identifies one or more receiving modules 210," Column 5 Lines 24 – 29) to identify each media channel to the plurality of processing modules (Column 6 Lines 24 – 26).

Claim 18: Borland discloses the integrated circuit claim 17, wherein the data path includes a control data path (control bus) to communicate processing control data to at least one processing module (modules 210), the control data path including a plurality of control channels (time slots) defined by time division multiplexed time-slots, wherein the channel identification path identifies both the media channels and the control channels (address bus includes identification information of the individual time slots corresponding to both the control and data buses) (Column 6 Lines 24 – 36).

Claim 20: Borland discloses the integrated circuit of claim 1, wherein the plurality of processing modules are digital audio processing modules selected from the group consisting of an audio memory transport module, a digital delay line module, a sample rate converter module, a filter module, a mixer module, a DSP module, and a digital Input/Output module (I/O controller, Column 4 Lines 1 – 4).

Claim 21: Borland discloses the integrated circuit of claim 1, wherein the integrated circuit is in a very large scale integration (VLSI) device (The integrated circuit 100 is a system-on-a-chip and therefore a VLSI device, Column 1 Lines 5 – 35).

Claim 22: Borland discloses a digital processing integrated circuit to process media data (integrated circuit 100 data transfers may be voice, audio, and/or video, Column 5 Lines 43 – 45 and Figures 1 – 3), the integrated circuit including: a plurality of processing modules to process the media data (modules 210A – 210H); a media data path to communicate the media data between adjacent processing modules; a processing control data path to communicate processing control data between the adjacent processing modules (two circular buses, 330 and 332), wherein the processing control data (transfer requests) defines processing functionality at an associated processing module (Transfer requests provide identifier information, transfer size, and timing information necessary for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36.) and wherein each processing module of the plurality of processing modules is configured to communicate the media data and the processing control data to an adjacent processing module (Since processing modules are arranged in a ring configuration the data must be passed to an adjacent processing module) and media data and processing control data is clocked from processing module to processing module around the data path so as to communicate the media data and the processing control data from a source processing module to a target processing module (Since the modules are serially connected the

modules and the bus is a TDMA bus, data is passed through all modules starting with the source however is only processed at the appropriate destination module, Column 1 Line 39 – Column 2 Line 44 and Column 5 Lines 55 – 59); the integrated circuit including a routing controller (bus controller 350) to route the media data and the processing control data along the data path to an associated processing module; and a digital interface to communicate media data with a device external to the integrated circuit (module 210 may be an I/O controller communicating with a computer system) (Column 1 Lines 5 – 35, Column 3 Line 64 – Column 4 Line 12).

Claim 23: Borland discloses the integrated circuit of claim 22, wherein while the media data is communicated from the source processing module to the target processing module, any one or more of the processing modules can add media data to or receive media data from the media data path (Processing modules perform operations and therefore receive media data from the media data path, process the media data, and then add the media data back to the media data path, Column 3 Line 64 – Column 4 Line 12).

Claim 24: Borland discloses a method to process media data in communicate media data a plurality of processing modules in a digital media processing integrated circuit (integrated circuit 100 data transfers may be voice, audio, and/or video, Column 5 Lines 43 – 45 and Figures 1 – 3), the method including: communicating, at each processing module within the integrated circuit (communicating via circular buses 330 and 332,

Figures 2 and 3), providing the media data from the processing module to an adjacent processing module along a data path (Since processing modules are arranged in a ring configuration the data must be passed to an adjacent processing module) interconnecting the plurality of processing modules (transfer requests) in a ring configuration until media data from a source processing module is received; extracting the media data at a target processing module of the plurality of processing modules (Since the modules are serially connected the modules and the bus is a TDMA bus, data is passed through all modules starting with the source however is only processed at the appropriate destination module, Column 1 Line 39 – Column 2 Line 44 and Column 5 Lines 55 – 59); and communicating media data between the data path and a device external to the integrated circuit (module 210 may be an I/O controller communicating with a computer system) (Column 1 Lines 5 – 35, Column 3 Line 64 – Column 4 Line 12).

Claim 25: Borland discloses the method of claim 24, which includes communicating the media data sequentially between the plurality of processing modules ("Buses 330 and 332 may be serial or parallel buses, as desired," Column 6 Lines 24 – 36).

Claim 26: Borland discloses the method of claim 24, wherein the data path includes a processing module identifier ("an identifier which identifies one or more receiving modules 210," Column 5 Lines 24 – 29) that identifies the source processing module

that provides the media to the data path (each module has an assigned time slot to communicate information, Column 5 Lines 55 – 59).

Claim 27: Borland discloses the method of claim 24, wherein media data received at a last processing module of the plurality of processing modules is communicated to first processing module of the plurality of processing modules. (Since the modules are serially connected the modules and the bus is a TDMA bus, data is passed through all modules however is only processed at the appropriate destination module, Column 1 Line 39 – Column 2 Line 44, The circular configuration also means that the last processing module must communicate information to the first processing module).

Claim 28: Borland discloses the method of claim 24, wherein the data path includes a plurality of time-slots (TDMA bus), the method including providing the processed media data into a time-slot associated with a source processing module (each module has an assigned time slot to communicate information, Column 5 Lines 55 – 59) and wherein data corresponding to different processing modules is present at the same time on the data path (Since this is TDMA system media data corresponding to different processing modules is present in different time slots or "at the same time" referring to absolute time, on the data path, Column 5 Lines 55 – 59).

Claim 29: Borland discloses the method of claim 24, wherein the data path includes a digital media path and a processing control path (buses 330 and 332), the method

including: providing the media data in the form of audio data ("voice, audio and/or video transfers," Column 5 Lines 44 – 45) to the digital media path; and providing processing control data to the processing control data path, the processing control data controlling the processing of the audio data by the target processing module (Transfer requests provide identifier information, transfer size, and timing information necessary for the processing module to process the digital data received from the data path, Column 5 Lines 24 – 36).

Claims 30 – 35: Claims 30 – 35 are substantially similar in scope to claims 3 – 8 and therefore are rejected for the same reasons.

Claims 36 – 46: Claims 36 – 46 are substantially similar in scope to claims 10 – 20 and therefore are rejected for the same reasons.

Claims 47 – 69: Claims 47 – 69 are substantially similar in scope to claims 24 – 46 and therefore are rejected for the same reasons.

Claim 70: Borland discloses the integrated circuit of claim 1, wherein each processing module includes an input to receive data (bus interface logic 410 and input buffer 420, Figure 7B) sent by a first adjacent processing module, and an output (bus interface logic 410 and output buffer 420, Figure 7B) to send data to a second adjacent processing module to allow serial interconnection of the processing modules in the ring

configuration (Since processing modules are arranged in a ring configuration the data must be passed to an adjacent processing module).

Claim 71: Borland discloses the integrated circuit of claim 70, wherein the input includes at least one input register (bus interface logic 410 input buffer 420) connected by the data path to the first adjacent processing module, and the output includes at least one output register (bus interface logic 410 output buffer 420) connected by the data path to the second adjacent processing module and media data is clocked along the data path by the at least one input register and the at least one output register (Media data is received from the bus into the input buffer of the processing module, processed, and then output from the output buffer onto the during the assigned TDMA time slot, Column 5 Lines 1 – 13 and Lines 5 – 59).

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borland et al. (US 6,724,772 B1).

Claim 19: Borland discloses the integrated circuit of claim 1, but *does not disclose* wherein the data path includes a transport bus to communicate data between an external memory that is separate from the integrated circuit and at least one of the

plurality of processing modules of the integrated circuit. Borland does disclose that one of the processing modules 210 is an I/O controller (Column 4 Line 2) and that the integrated circuit processes audio data (Column 6 Line 44). Borland also discloses that computer systems comprise a motherboard, microprocessor, memory, and busses, and also a plurality of computer chips. Borland then discloses that the integrated circuit simplifies the amount of computer chips necessary by combining the components into a single integrated circuit, which results in a system-on-a-chip (SOC) (Column 1 Lines 5 – 35). Therefore, since the system-on-a-chip is within a computer system and the SOC is responsible for processing media data it would have been obvious to one of ordinary skill in the art at the time of the invention to use the I/O controller of the integrated circuit and the buses located within the computer system to transfer media data from a memory, which commonly holds media data within a computer system, on the bus within the computer system to the I/O of the integrated circuit, so that the integrated circuit can have a source of media to process.

Response to Arguments

9. Applicant's arguments filed June 7, 2007 have been fully considered but they are not persuasive. The claims call for the media data path to interconnect the plurality of processing modules in series. In Figures 2 and 3 Borland clearly discloses bus 330 and describes bus 330 as being a data bus. Bus 332 of Figure 2 and also the connections between bus controller 350 and the processing modules in Figure 3 are described as a control bus. Therefore, although the processing modules have parallel connections to

the bus controller, the data bus interconnects the plurality of processing modules in series. Contrary to the Applicant's interpretation of the reference, if the media data bus 330 is severed communication of media data will not take place since media data cannot be communicated on the control bus.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Saunders whose telephone number is (571) 270-1063. The examiner can normally be reached on Monday - Thursday, 9:00 a.m. - 4:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
August 14, 2007

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SUPERVISORY PATENT EXAMINER